CLAIMS:

1. A power limiter comprising input terminals and a transmission line arranged to couple a high frequency signal supplied to the input terminals to an output of the limiter, the transmission line comprising a plurality of successive transmission line sections each comprising at least a series inductance and a shunt capacitance, the shunt capacitance comprising a capacitance of at least one diode connected to an output of the respective transmission line section to limit voltage of said signal at said output of the respective transmission line section.

2. A limiter as claimed in claim 1 wherein said at least one diode comprises at least two oppositely poled diodes connected in parallel at the output of the respective transmission line section.

3. A limiter as claimed in claim 1 wherein said at least one diode of at least one of the transmission line sections comprises a plurality of diodes connected in series.

4. A limiter as claimed in claim 3 wherein different ones of said transmission line sections have different numbers of diodes constituting said at least one diode of the respective transmission line sections, said numbers decreasing from the input terminals towards the output of the limiter.

5. A limiter as claimed in claim 1 wherein said at least one diode of at least one of the transmission line sections comprises an array of a plurality of parallel-connected sets of diodes, each set comprising a plurality of diodes connected in series.

6. A limiter as claimed in claim 5 wherein said array of at least one of the transmission line sections comprises a square array of diodes.

7. A limiter as claimed in claim 5 wherein different ones of said transmission line sections have different numbers of diodes constituting said at least one diode of the respective transmission line sections, said numbers decreasing from the input terminals towards the output of the limiter.

8. A limiter as claimed in claim 2 wherein each of said at least two oppositely poled diodes of at least one of the transmission line sections comprises a plurality of diodes connected in series.

9. A limiter as claimed in claim 8 wherein different ones of said transmission line sections have different numbers of diodes constituting each of said at least two oppositely poled diodes of the respective transmission line sections, said numbers decreasing from the input terminals towards the output of the limiter.

10. A limiter as claimed in claim 2 wherein each of said at least two oppositely poled diodes of at least one of the transmission line sections comprises an array of a plurality of parallel-connected sets of diodes, each set comprising a plurality of diodes connected in series.

11. A limiter as claimed in claim 10 wherein said arrays of at least one of the transmission line sections comprise square arrays of diodes.

12. A limiter as claimed in claim 10 wherein different ones of said transmission line sections have different numbers of diodes constituting each of said at least two oppositely

poled diodes of the respective transmission line sections, said numbers decreasing from the input terminals towards the output of the limiter.

13. A limiter as claimed in claim 12 wherein there are four transmission line sections with, respectively a square array of 16 diodes, a square array of 9 diodes, a square array of 4 diodes, and 1 diode constituting each of said at least two oppositely poled diodes of the respective transmission line sections.

14. A limiter as claimed in claim 1 wherein each diode comprises a MESFET having a source and drain connected together.

15. An integrated circuit device comprising a limiter as claimed in claim 1 and a high frequency circuit having an input coupled to the output of the limiter.

16. An integrated circuit device as claimed in claim 15 wherein the high frequency circuit comprises an amplifier.

17. An integrated circuit device as claimed in claim 15 wherein the device comprises a gallium arsenide integrated circuit device.

18. A high frequency signal power limiter comprising a plurality of transmission line sections connected in succession, each transmission line section comprising:

two input connections;

two output connections;

at least one inductance coupling the two input connections to the two output connections; and

at least two oppositely-poled diodes coupled between the two output connections.

19. A limiter as claimed in claim 18 wherein each of said at least two oppositely poled diodes of each of the successive transmission line sections except a last one of the successive transmission line sections comprises a plurality of diodes connected in series, a number of said plurality of diodes connected in series decreasing for the successive transmission line sections towards said last one of the successive transmission line sections.

20. A limiter as claimed in claim 18 wherein each of said at least two oppositely poled diodes of each of the successive transmission line sections except a last one of the successive transmission line sections comprises an array of a plurality of parallel-connected sets of diodes, each set comprising a plurality of diodes connected in series, a number of said plurality of diodes connected in series decreasing for the successive transmission line sections towards said last one of the successive transmission line sections.

21. A limiter as claimed in claim 20 wherein each array comprises a square array of diodes.

22. A limiter as claimed in claim 18 wherein each diode comprises a MESFET having a source and drain connected together.

23. A gallium arsenide integrated circuit comprising a limiter as claimed in claim 18 and a high frequency circuit having an input coupled to an output of the limiter.

24. A limiter comprising a plurality of transmission line sections connected in succession, each transmission line section comprising at least one series inductance coupling an input to an output of the transmission line section, and at least one

shunt diode coupled at the output of the transmission line section to limit voltage of said signal at said output.